Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): A method of determining a DC margin of a latch of a circuit, the circuit including one or more circuit elements, and the latch including a plurality of signal paths for passing signals through the one or more circuit elements, the method comprising:

determining a worst case pull-up path and a worst case pull-down path analytically by accumulating a weighted resistance of each circuit element along the plurality of signal paths, wherein weights assigned to the circuit elements are empirically determined based on a topology configuration of each of the circuit elements, and wherein the topology configuration includes one or more of a type of the circuit elements, the signals being passed through the circuit elements, and whether a threshold voltage drop occurs between a drive circuit element and a pass circuit element;

performing a first simulation using a first simulation circuit to determine a trip voltage of a forward inverter of said latch;

performing a second simulation using a second simulation circuit to determine a one margin of said latch, said second simulation circuit comprising ~~a~~ the worst case pull-up signal path; and

performing a third simulation using a third simulation circuit to determine a zero margin of said latch, said third simulation circuit comprising ~~a~~ the worst case pull-down signal path.

2. (original): The method of determining a DC margin of a latch in accordance with claim 1, further comprising:

determining said worst case pull-up signal path analytically by comparing a cumulative weighted resistance of at least one pull-up signal path to said latch.

3. (original): The method of determining a DC margin of a latch in accordance with claim 2, wherein said step of determining said worst case pull-up signal path comprises:

identifying one or more pass circuit elements along each of possible pull-up signal paths;

determining a resistance of each of said identified one or more pass circuit elements based on respective sizes of said identified one or more pass circuit elements;

applying to said resistance, of each of said identified one or more pass circuit elements, a weight based on topology configuration of a corresponding one of said identified one or more pass circuit elements to produce one or more weighted resistance;

summing said one or more weighted resistance to produce said cumulative weighted resistance of each of said possible pull-up signal paths; and

determining said worst case pull-up signal path having a highest cumulative weighted resistance among said possible pull-up signal paths.

4. (original): The method of determining a DC margin of a latch in accordance with claim 1, further comprising:

determining said worst case pull-down signal path analytically by comparing a cumulative weighted resistance of at least one pull-down signal path to said latch.

5. (original): The method of determining a DC margin of a latch in accordance with claim 4, wherein said step of determining said worst case pull-down signal path comprises:

identifying one or more pass circuit elements along each of possible pull-down signal paths;

determining a resistance of each of said identified one or more pass circuit elements based on respective sizes of said identified one or more pass circuit elements;

applying to said resistance, of each of said identified one or more pass circuit elements, a weight based on topology configuration of a corresponding one of said identified one or more pass circuit elements to produce one or more weighted resistance;

summing said one or more weighted resistance to produce said cumulative weighted resistance of each of said possible pull-down signal paths; and

determining said worst case pull-down signal path having a highest cumulative weighted resistance among said possible pull-down signal paths.

6. (original): The method of determining a DC margin of a latch in accordance with claim 1, wherein said step of performing said second simulation comprises:

setting an initial value of an output, of a portion of said second simulation circuit representing said latch, to a logical high;

applying a logical high pull-up input signal to an input, of said portion of said second simulation circuit representing said latch, through said worst case pull-up signal path; and

determining a voltage level at said input.

7. (original): The method of determining a DC margin of a latch in accordance with claim 1, wherein said step of performing said third simulation comprises:

setting an initial value of an output, of a portion of said third simulation circuit representing said latch, to a logical low;

applying a logical low pull-down input signal to an input, of said portion of said third simulation circuit representing said latch, through said worst case pull-down signal path; and

determining a voltage level at said input.

8. (currently amended): A computer readable storage medium having stored thereon computer program for implementing a method of determining a DC margin of a latch of a circuit, the circuit including one or more circuit elements, and the latch including a plurality of signal paths for passing signals through the one or more circuit elements, said computer program comprising a set of instructions for:

determining a worst case pull-up path and a worst case pull-down path analytically by accumulating a weighted resistance of each circuit element along the plurality of signal paths, wherein weights assigned to the circuit elements are empirically determined based on a topology configuration of each of the circuit elements, and wherein the topology configuration includes one or more of a type of the circuit elements, the signals being passed through the circuit elements, and whether a threshold voltage drop occurs between a drive circuit element and a pass circuit element;

performing a first simulation using a first simulation circuit to determine a trip voltage of a forward inverter of said latch;

performing a second simulation using a second simulation circuit to determine a one margin of said latch, said second simulation circuit comprising ~~a~~ the worst case pull-up signal path; and

performing a third simulation using a third simulation circuit to determine a zero margin of said latch, said third simulation circuit comprising ~~a~~ the worst case pull-down signal path .

9. (original): The computer readable storage medium according to claim 8, wherein said computer program further comprising one or more instructions for:

determining said worst case pull-up signal path analytically by comparing a cumulative weighted resistance of at least one pull-up signal path to said latch.

10. (original): The computer readable storage medium according to claim 9, wherein said computer program further comprising one or more instructions for:

identifying one or more pass circuit elements along each of possible pull-up signal paths;

determining a resistance of each of said identified one or more pass circuit elements based on respective sizes of said identified one or more pass circuit elements;

applying to said resistance, of each of said identified one or more pass circuit elements, a weight based on topology configuration of a corresponding one of said identified one or more pass circuit elements to produce one or more weighted resistance;

summing said one or more weighted resistance to produce said cumulative weighted resistance of each of said possible pull-up signal paths; and

determining said worst case pull-up signal path having a highest cumulative weighted resistance among said possible pull-up signal paths.

11. (original): The computer readable storage medium according to claim 8, wherein said computer program further comprising one or more instructions for:

determining said worst case pull-down signal path analytically by comparing a cumulative weighted resistance of at least one pull-down signal path to said latch.

12. (original): The computer readable storage medium according to claim 11, wherein said computer program further comprising one or more instructions for:

identifying one or more pass circuit elements along each of possible pull-down signal paths;

determining a resistance of each of said identified one or more pass circuit elements based on respective sizes of said identified one or more pass circuit elements;

applying to said resistance, of each of said identified one or more pass circuit elements, a weight based on topology configuration of a corresponding one of said identified one or more pass circuit elements to produce one or more weighted resistance;

summing said one or more weighted resistance to produce said cumulative weighted resistance of each of said possible pull-down signal paths; and

determining said worst case pull-down signal path having a highest cumulative weighted resistance among said possible pull-down signal paths.

13. (original): The computer readable storage medium according to claim 8, wherein said one or more instructions for performing said second simulation comprises one or more instructions for:

setting an initial value of an output, of a portion of said second simulation circuit representing said latch, to a logical high;

applying a logical high pull-up input signal to an input, of said portion of said second simulation circuit representing said latch, through said worst case pull-up signal path; and

determining a voltage level at said input.

14. (original): The computer readable storage medium according to claim 8, wherein said one or more instructions for performing said third simulation comprises one or more instructions for:

setting an initial value of an output, of a portion of said second simulation circuit representing said latch, to a logical low;

applying a logical low pull-down input signal to an input, of said portion of said second simulation circuit representing said latch, through said worst case pull-down signal path; and

determining a voltage level at said input.

15. (currently amended): A simulation circuit for determining a DC margin of a latch of a circuit, the circuit including one or more circuit elements, and the latch including a plurality of signal paths for passing signals through the one or more circuit elements, comprising:

a latch portion representing said latch being simulated, said latch portion comprising a forward inverter and a feedback inverter, an input of said forward inverter being operably connected to an input of said latch portion, and an input of said feedback inverter being operably connected to an output of said latch portion;

a driver portion representing a driver circuit element capable of supplying an input signal to said latch being simulated; and

a pass path subcircuit configured to receive a drive signal from said driver portion, and configured to supply said drive signal to said input of said latch portion, said pass path subcircuit representing one or more pass circuit elements along a worst case signal path between said driver circuit element and said latch being simulated,

wherein the worst case signal path is determined analytically by accumulating a weighted resistance of each circuit element along the plurality of signal paths, wherein weights assigned to the circuit elements are empirically determined based on a topology configuration of each of the circuit elements, and wherein the topology configuration includes one or more of a type of the circuit elements, the signals being passed through the circuit elements, and whether a threshold voltage drop occurs between a drive circuit element and a pass circuit element.

16. (original): The simulation circuit according to claim 15, wherein each of said forward inverter and said feedback inverter comprises:

a complementary pair of field effect transistors.

17. (original): The simulation circuit according to claim 15, wherein said pass path subcircuit comprises:

one or more field effect transistors.

18. (original): The simulation circuit according to claim 17, wherein:

at least two of said one or more field effect transistors are arranged as a complementary pair.

19. (original): The simulation circuit according to claim 17, wherein:

each of said one or more field effect transistors representing corresponding one of said one or more pass circuit elements along a worst case signal path between said driver circuit element and said latch being simulated; and

wherein sizes of said one or more field effect transistors are chosen based on respective resistance of corresponding ones of said one or more pass circuit element.

20. (cancelled).